Rad-Hard, 5.0V/3.3V µ-Processor Supervisory Circuits

ISL705AEH, ISL705BEH, ISL705CEH, ISL706AEH, ISL706BEH, ISL706CEH

This family of devices are radiation hardened 5.0V/3.3V supervisory circuits that reduce the complexity required to monitor supply voltages in microprocessor systems. These devices significantly improve accuracy and reliability relative to discrete solutions. Each IC provides four key functions.

1. A reset output during power-up, power-down, and brownout conditions.
2. An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6s.
3. A precision threshold detector for monitoring a power supply other than V_{DD}.
4. An active-low manual-reset input.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table on page 3 must be used when ordering.

Detailed Electrical Specifications for the ISL705AEH, ISL705BEH, ISL705CEH, ISL706AEH, ISL706BEH and ISL706CEH are contained in SMD 5962-11213. A "hot-link" is also provided on our website for downloading.

Applications

- Supervisor for µ-Processors, µ-Controllers, FPGAs and DSPs
- Critical Power Supply Monitoring
- Reliable Replacement of Discrete Solutions

Features

- Electrically Screened to SMD 5962-11213
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardness
  - High Dose Rate. . . . . 100krad(Si)
  - Low Dose Rate . . . . . 100krad(Si) (Note 1)
  - SEL/SEB LET_{TH}. . . . . 86MeV * cm^2/mg
- Precision Supply Voltage Monitor
  - 4.65V Threshold in the ISL705AEH/BEH/CEH
  - 3.08V Threshold in the ISL706AEH/BEH/CEH
- 200ms (Typ) Reset Pulse Width
  - Active High, Active Low and Open Drain Options
- Independent Watchdog Timer with 1.6s (Typ) Timeout
- Precision Threshold Detector
  - 1.25V Threshold in the ISL705AEH/BEH/CEH
  - 0.6V Threshold in the ISL706AEH/BEH/CEH
- Debounced TTL/CMOS Compatible Manual-Reset Input
- Reset Output Valid at V_{DD} = 1.2V

Related Literature

- AN1650, "ISL705XRH Evaluation Board User's Guide"
- AN1671, "ISL706xRH Evaluation Board User's Guide"
- AN1651, "Single Event Effects (SEE) Testing of the ISL705xRH/EH and ISL706xRH/EH Rad Hard Supervisory Circuits"

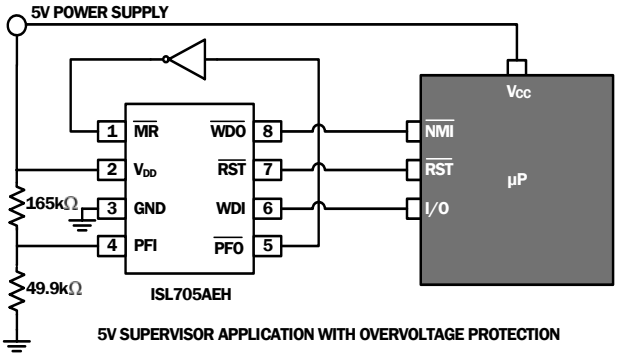


FIGURE 1. TYPICAL APPLICATION

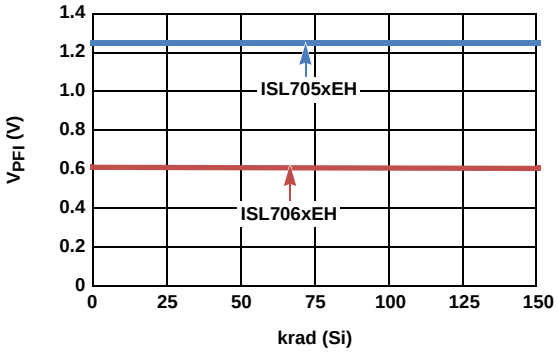


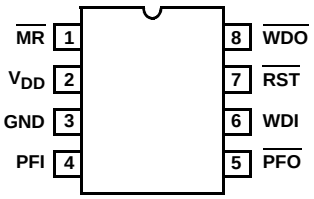
FIGURE 2. PRECISION THRESHOLD DETECTOR LOW DOSE IONIZING CHARACTERISTIC CURVE

NOTE:

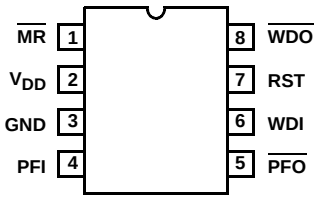
1. Product capability established by initial characterization. The EH version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate.

Pin Configurations

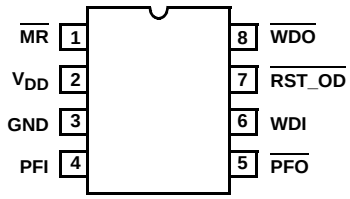
ISL705AEH, ISL706AEH
(8 LD FLATPACK)
TOP VIEW



ISL705BEH, ISL706BEH
(8 LD FLATPACK)
TOP VIEW



ISL705CEH, ISL706CEH
(8 LD FLATPACK)
TOP VIEW



Pin Descriptions

ISL705AEH ISL706AEH	ISL705BEH ISL706BEH	ISL705CEH ISL706CEH	NAME	DESCRIPTION
1	1	1	$\overline{MR}$	**Manual Reset.** $\overline{MR}$ is an active-low, debounced, TTL/CMOS compatible input that may be used to trigger a reset pulse.
2	2	2	V_{DD}	**Power Supply.** V_{DD} is a supply voltage input that provides power to all internal circuitry. This input is also monitored and used to trigger a reset pulse. Reset is guaranteed operable after V_{DD} rises above 1.2V.
3	3	3	GND	**Ground.** GND is a supply voltage return for all internal circuitry. This return establishes the reference level for voltage detection and should be connected to signal ground.
4	4	4	PFI	**Power Fail Input**. PFI is an input to a threshold detector, which may be used to monitor another supply voltage level. The threshold of the detector (V_{PFI}) is 1.25V in the ISL705AEH/BEH/CEH and 0.6V in the ISL706AEH/BEH/CEH.
5	5	5	$\overline{PFO}$	**Power Fail Output.** $\overline{PFO}$ is an active-low, push-pull output of a threshold detector that indicates the voltage at the PFI pin is less than V_{PFI}.
6	6	6	WDI	**Watchdog Input.** WDI is a tri-state input that monitors microprocessor activity. If the microprocessor does not toggle WDI within 1.6s and WDI is not tri-stated, $\overline{WDO}$ goes low. As long as reset is asserted or WDI is tri-stated, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Floating WDI or connecting WDI to a high impedance tri-state buffer disables the watchdog feature.
7	-	-	$\overline{RST}$	**Reset**. $\overline{RST}$ is an active-low, push-pull output that is guaranteed to be low once V_{DD} reaches 1.2V. As V_{DD} rises, $\overline{RST}$ stays low. When V_{DD} rises above a 4.65V (ISL705AEH/BEH/CEH) or 3.08V (ISL706AEH/BEH/CEH) reset threshold, an internal timer releases $\overline{RST}$ after about 200ms. $\overline{RST}$ pulses low whenever V_{DD} goes below the reset threshold. If a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse will continue for at least 140ms. On power-down, once V_{DD} falls below the reset threshold, $\overline{RST}$ goes low and is guaranteed low until V_{DD} drops below 1.2V.
-	7	-	RST	**Reset.** RST is an active-high, push-pull output. RST is the inverse of $\overline{RST}$.
-	-	7	$\overline{RST\_OD}$	**Reset.** $\overline{RST\_OD}$ is an active-low, open-drain output that goes low when reset is asserted. This pin may be pulled up to V_{DD} with a resistor consistent with the sink and leakage current specifications of the output. Behavior is otherwise identical to the $\overline{RST}$ pin.
8	8	8	$\overline{WDO}$	**Watchdog Output.** $\overline{WDO}$ is an active-low, push-pull output that goes low if the microprocessor does not toggle WDI within 1.6s and WDI is not tri-stated. $\overline{WDO}$ is usually connected to the non-maskable interrupt input of a microprocessor. When V_{DD} drops below the reset threshold, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out. Reset is simultaneously asserted, thus preventing an interrupt. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{DD} drops below the reset threshold, thus functioning as a low line output.

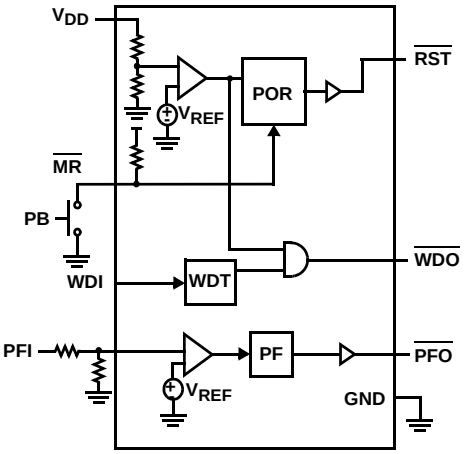
Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP RANGE (°C)	PACKAGE (RoHs Compliant)	PKG. DWG. #
5962R1121307VXC	ISL705AEHVF (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
5962R1121307V9A	ISL705AEHVX	-55 to +125	Die	
ISL705ARHF/PROTO	ISL705ARHF/PROTO (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
ISL705ARHX/SAMPLE	ISL705ARHX/SAMPLE	-55 to +125	Die	
5962R1121308VXC	ISL705BEHVF (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
5962R1121308V9A	ISL705BEHVX	-55 to +125	Die	
ISL705BRHF/PROTO	ISL705BRHF/PROTO (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
ISL705BRHX/SAMPLE	ISL705BRHX/SAMPLE	-55 to +125	Die	
5962R1121309VXC	ISL705CEHVF (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
5962R1121309V9A	ISL705CEHVX	-55 to +125	Die	
ISL705CRHF/PROTO	ISL705CRHF/PROTO (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
ISL705CRHX/SAMPLE	ISL705CRHX/SAMPLE	-55 to +125	Die	
5962R1121310VXC	ISL706AEHVF (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
5962R1121310V9A	ISL706AEHVX	-55 to +125	Die	
ISL706ARHF/PROTO	ISL706ARHF/PROTO (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
ISL706ARHX/SAMPLE	ISL706ARHX/SAMPLE	-55 to +125	Die	
5962R1121311VXC	ISL706BEHVF (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
5962R1121311V9A	ISL706BEHVX	-55 to +125	Die	
ISL706BRHF/PROTO	ISL706BRHF/PROTO (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
ISL706BRHX/SAMPLE	ISL706BRHX/SAMPLE	-55 to +125	Die	
5962R1121312VXC	ISL706CEHVF (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
5962R1121312V9A	ISL706CEHVX	-55 to +125	Die	
ISL706CRHF/PROTO	ISL706CRHF/PROTO (Note 2)	-55 to +125	8 Ld Flatpack	K8.A
ISL706CRHX/SAMPLE	ISL706CRHX/SAMPLE	-55 to +125	Die	
ISL705XRHEVAL1Z	ISL705XRH Evaluation Board			
ISL706XRHEVAL1Z	ISL706XRH Evaluation Board			

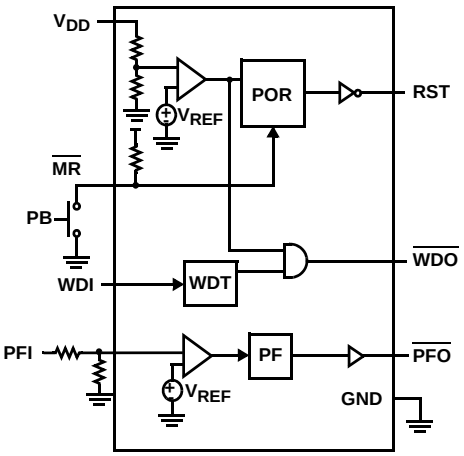
NOTE:

2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

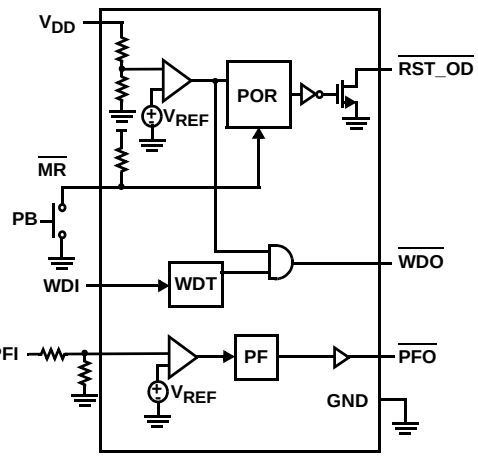
Functional Block Diagrams



ISL705AEH, ISL706AEH



ISL705BEH, ISL706BEH



ISL705CEH, ISL706CEH

Timing Diagrams

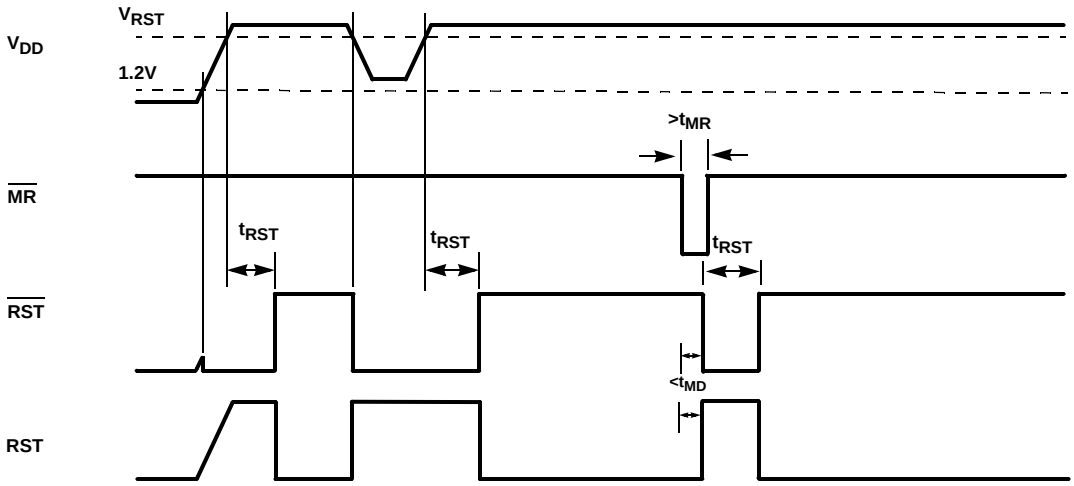


FIGURE 3. RST, $\overline{RST}$, $\overline{MR}$ AND $\overline{WDO}$ TIMING DIAGRAM

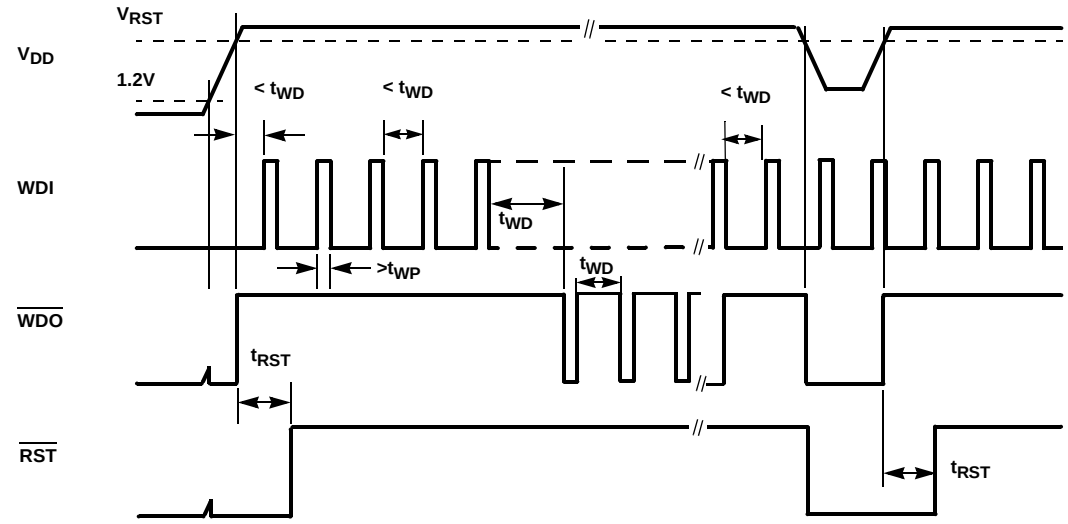


FIGURE 4. WATCHDOG TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage Range . . . . . -0.3V to 6.5V
Voltage on All Other Inputs . . . . . -0.3V to V_{DD} + 0.3V
ESD Rating
Human Body Model (Tested per MIL-PRF-883 3015.7). 3.0kV
Machine Model (Tested per JESD22-A115C) 300V
Charged Device Model (Tested per JESD22-C110D) 1.0kV
Latch Up (Tested per JESD-78C) . . . . . Class 2, Level A

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 3, 4).	140	15

Maximum Junction Temperature . . . . . +175°C
Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Temperature . . . . . -55°C to +125°C
Supply Voltage
ISL705AEH/BEH/CEH . . . . . 4.75V to 5.5V
ISL706AEH/BEH/CEH . . . . . 3.15V to 3.6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications

Unless otherwise specified V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = -55°C to +125°C. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 5)	TYP (Note 6)	MAX (Note 5)	UNITS
POWER SUPPLY SECTION						
V_{DD}	Operating Supply Voltage (Note 7)	ISL705AEH/BEH/CEH	**1.2**	5	**5.5**	V
		ISL706AEH/BEH/CEH	**1.2**	3.3	**3.6**	V
I_{DD}	Operating Supply Current	ISL705AEH/BEH/CEH			**530**	µA
		ISL706AEH/BEH/CEH			**400**	µA
RESET SECTION						
V_{RST}	Reset Threshold Voltage	ISL705AEH/BEH/CEH	**4.50**	4.65	**4.75**	V
		ISL706AEH/BEH/CEH	**3.00**	3.08	**3.15**	V
V_{HYS}	Reset Threshold Voltage Hysteresis	ISL705AEH/BEH/CEH	**20**	40		mV
		ISL706AEH/BEH/CEH	**20**	30		mV
t_{RST}	Reset Pulse Width		**140**	200	**280**	ms
V_{OUT}	Reset Output Voltage	ISL705AEH/BEH, I_{SOURCE} = 800µA	**V_{DD} - 1.5**			V
		ISL705AEH/BEH/CEH, I_{SINK} = 3.2mA			**0.4**	V
		ISL706AEH/BEH, I_{SOURCE} = 500µA	**0.8 x V_{DD}**			V
		ISL706AEH/BEH/CEH, I_{SINK} = 1.2mA			**0.3**	V
		ISL70XAEH/CEH, V_{DD} = 1.2V, I_{SINK} = 100µA			**0.3**	V
		ISL70XBEH, V_{DD} = 1.2V, I_{SOURCE} = 4µA	**0.9**			V
I_{LEAK}	Reset Output Leakage Current	ISL705CEH, V_{OUT} = V_{DD}			**1**	µA
		ISL706CEH, V_{OUT} = V_{DD}			**1**	µA

Electrical Specifications Unless otherwise specified V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = -55°C to +125°C. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 5)	TYP (Note 6)	MAX (Note 5)	UNITS
WATCHDOG SECTION						
t_{WD}	Watchdog Time-Out Period		**1.00**	1.60	**2.25**	s
t_{WP}	Watchdog Input (WDI) Pulse Width	ISL705AEH/BEH/CEH, V_{IL} = 0.4V, V_{IH} = 0.8 x V_{DD}	**50**			ns
		ISL706AEH/BEH/CEH, V_{IL} = 0.4V, V_{IH} = 0.8 x V_{DD}	**100**			ns
V_{IL}	Watchdog Input (WDI) Threshold Voltage	ISL705AEH/BEH/CEH			**0.8**	V
V_{IH}		ISL705AEH/BEH/CEH	**3.5**			V
V_{IL}		ISL706AEH/BEH/CEH			**0.6**	V
V_{IH}		ISL706AEH/BEH/CEH	**0.7 x V_{DD}**			V
I_{WDI}	Watchdog Input (WDI) Current	ISL705AEH/BEH/CEH, WDI = V_{DD}			**100**	µA
		ISL705AEH/BEH/CEH, WDI = 0V	**-100**			µA
		ISL706AEH/BEH/CEH, WDI = V_{DD}			**5**	µA
		ISL706AEH/BEH/CEH, WDI = 0V	**-5**			µA
V_{WDO}	Watchdog Output ($\overline{WDO}$) Voltage	ISL705AEH/BEH/CEH, I_{SOURCE} = 800µA	**V_{DD} - 1.5**			V
		ISL705AEH/BEH/CEH, I_{SINK} = 1.2mA			**0.4**	V
		ISL706AEH/BEH/CEH, I_{SOURCE} = 500µA	**0.8 x V_{DD}**			V
		ISL706AEH/BEH/CEH, I_{SINK} = 500µA			**0.3**	V
MANUAL RESET SECTION						
I_{MR}	Manual Reset ($\overline{MR}$) Pull-up Current	ISL705AEH/BEH/CEH, $\overline{MR}$ = 0V	**-500**		**-100**	µA
		ISL706AEH/BEH/CEH, $\overline{MR}$ = 0V	**-250**		**-25**	µA
t_{MR}	Manual Reset ($\overline{MR}$) Pulse Width	ISL705AEH/BEH/CEH	**150**			ns
		ISL706AEH/BEH/CEH	**150**			ns
V_{IL}	Manual Reset ($\overline{MR}$) Input Threshold Voltage	ISL705AEH/BEH/CEH			**0.8**	V
V_{IH}			**2.0**			V
V_{IL}		ISL706AEH/BEH/CEH			**0.6**	V
V_{IH}			**0.7 x V_{DD}**			V
t_{MD}	Manual Reset ($\overline{MR}$) to Reset Out Delay	ISL705AEH/BEH/CEH			**100**	ns
		ISL706AEH/BEH/CEH			**100**	ns
THRESHOLD DETECTOR SECTION						
V_{PFI}	Power Fail Input (PFI) Input Threshold Voltage	ISL705AEH/BEH/CEH	**1.20**	1.25	**1.30**	V
		ISL706AEH/BEH/CEH	**0.576**	0.6	**0.624**	V
I_{PFI}	Power Fail Input (PFI) Input Current		**-10**		**10**	nA
V_{PFO}	Power Fail Output (PFO) Output Voltage	ISL705AEH/BEH/CEH, I_{SOURCE} = 800µA	**V_{DD} - 1.5**			V
		ISL705AEH/BEH/CEH, I_{SINK} = 3.2mA			**0.4**	V
		ISL706AEH/BEH/CEH, I_{SOURCE} = 500µA	**0.8 x V_{DD}**			V
		ISL706AEH/BEH/CEH, I_{SINK} = 1.2mA			**0.3**	V
t_{RPFI}	PFI Rising Threshold Crossing to PFO Delay	ISL705AEH/BEH/CEH		7	**15**	µs
		ISL706AEH/BEH/CEH		11	**20**	µs

Electrical Specifications Unless otherwise specified V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = -55°C to +125°C. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 5)	TYP (Note 6)	MAX (Note 5)	UNITS
t_{FPFI}	PFI Falling Threshold Crossing to PFO Delay	ISL705AEH/BEH/CEH		20	**35**	µs
		ISL706AEH/BEH/CEH		25	**40**	µs

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Typical values shown reflect $T_A = T_J$ = +25°C operation and are not guaranteed.
7. Reset is the only parameter operable within 1.2V and the minimum recommended operating supply voltage.

Typical Performance Curves

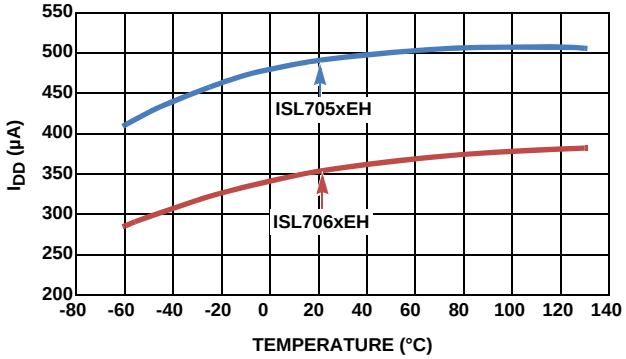


FIGURE 5. I_{DD} vs TEMPERATURE

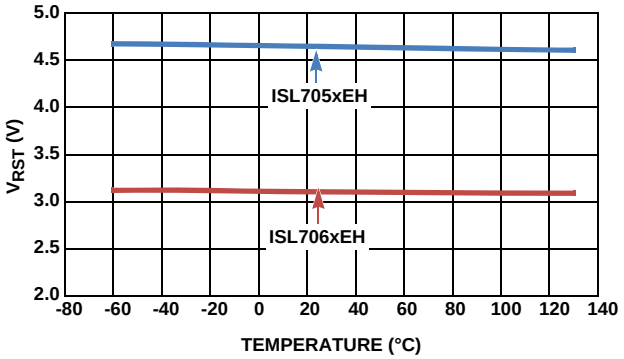


FIGURE 6. V_{RST} vs TEMPERATURE

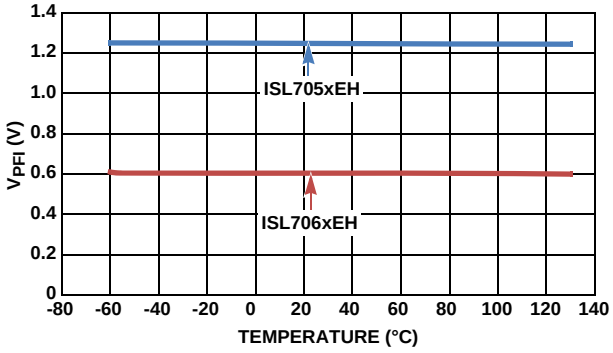


FIGURE 7. V_{PFI} vs TEMPERATURE

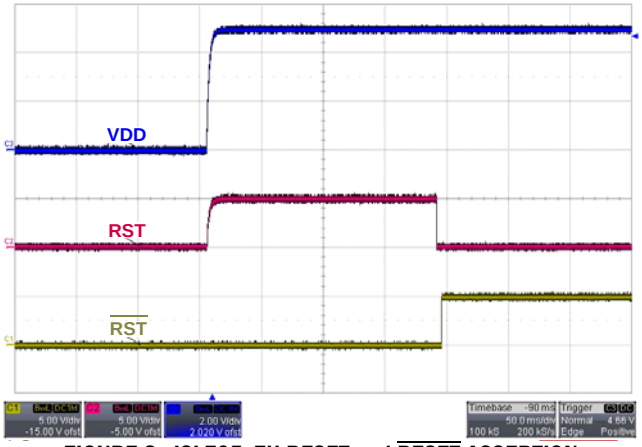


FIGURE 8. ISL705xEH RESET and $\overline{\text{RESET}}$ ASSERTION

Typical Performance Curves (Continued)

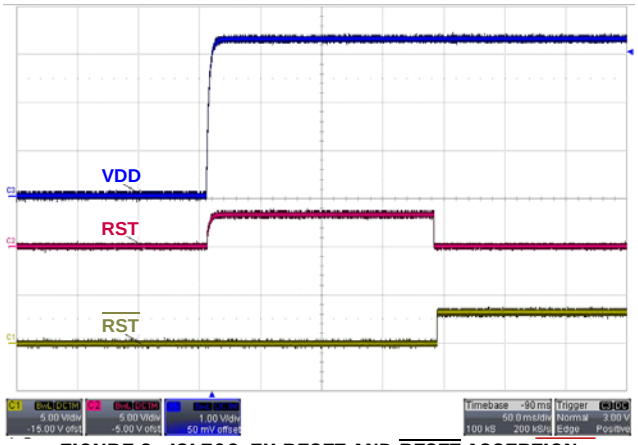


FIGURE 9. ISL706xEH RESET AND $\overline{\text{RESET}}$ ASSERTION

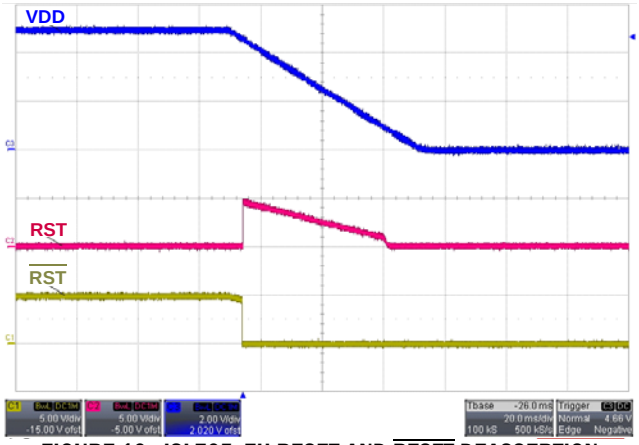


FIGURE 10. ISL705xEH RESET AND $\overline{\text{RESET}}$ DEASSERTION

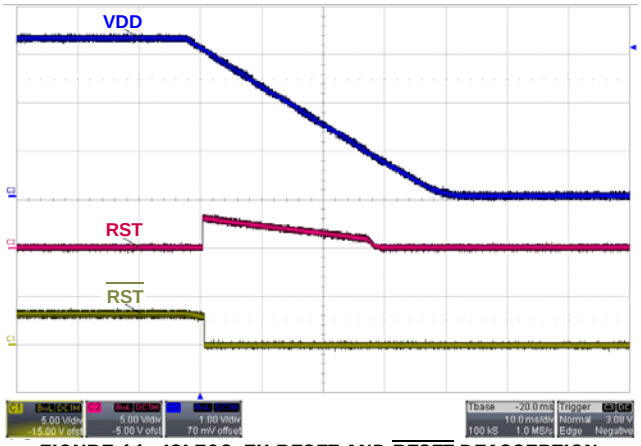


FIGURE 11. ISL706xEH RESET AND $\overline{\text{RESET}}$ DEASSERTION

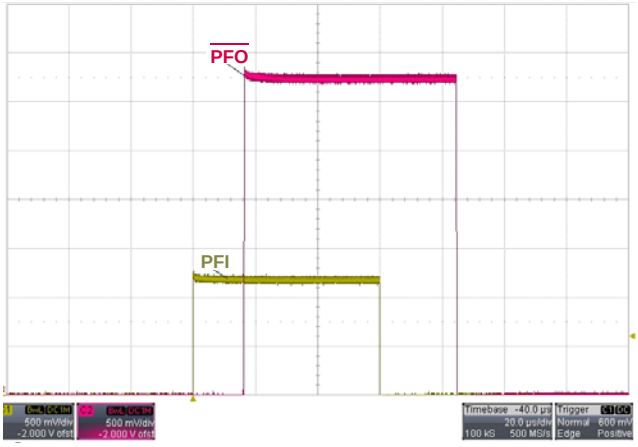


FIGURE 12. ISL705xEH PFI TO PFO RESPONSE

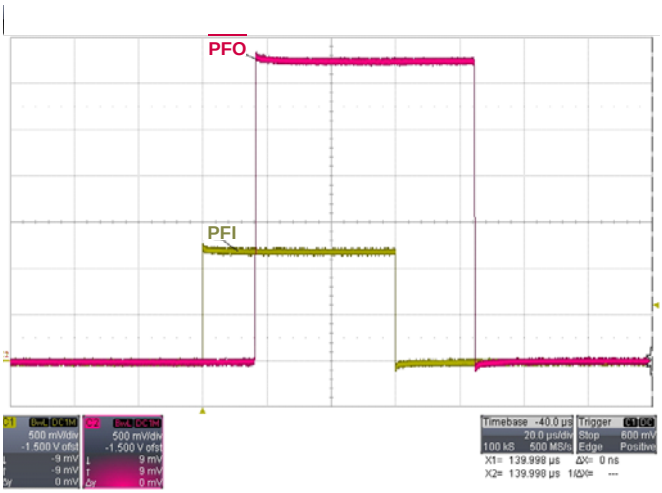


FIGURE 13. ISL706xEH PFI TO PFO RESPONSE

Post Radiation Characteristics Unless otherwise specified, V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = +25°C. **This data is parameter deltas post radiation exposure at a rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.**

SYMBOL	PARAMETER	CONDITIONS	0 - 25kRad	0 - 50kRad	0 - 75kRad	0 - 100kRad	UNITS
POWER SUPPLY SECTION							
I_{DD}	Operating Supply Current	ISL705AEH/BEH/CEH	-2	-2.44	-3.86	-4.88	µA
		ISL706AEH/BEH/CEH	-4.79	-7.47	-6.93	-8.88	µA
RESET SECTION							
V_{RST}	Reset Threshold Voltage	ISL705AEH/BEH/CEH	-8.1	-13.1	-17.5	-18.1	mV
		ISL706AEH/BEH/CEH	-1	-3.25	-5.38	-7.25	mV
V_{HYS}	Reset Threshold Voltage Hysteresis	ISL705AEH/BEH/CEH	-3.75	-1.9	-5	-3.12	mV
		ISL706AEH/BEH/CEH	0.375	0.25	0.625	0.625	mV
t_{RST}	Reset Pulse Width		-2.13	-2.18	-2.39	-2.35	ms
WATCHDOG SECTION							
t_{WD}	Watchdog Time-Out Period		-56	-72	-81	-80	ms
MANUAL RESET SECTION							
t_{MD}	Manual Reset ($\overline{MR}$) to Reset Out Delay	ISL705AEH/BEH/CEH	0.028	0.146	0.274	0.368	ns
		ISL706AEH/BEH/CEH	0.305	0.605	0.793	0.956	ns
THRESHOLD DETECTOR SECTION							
V_{PFI}	Power Fail Input (PFI) Input Threshold Voltage	ISL705AEH/BEH/CEH	0.94	0.31	0	-0.62	mV
		ISL706AEH/BEH/CEH	-1.56	-2.5	-2.5	-2.5	mV
t_{RPFI}	PFI Rising Threshold Crossing to PFO Delay	ISL705AEH/BEH/CEH	-0.026	-0.047	-0.085	-0.068	µs
		ISL706AEH/BEH/CEH	0.028	-0.058	0.11	-0.11	µs
t_{FPFI}	PFI Falling Threshold Crossing to PFO Delay	ISL705AEH/BEH/CEH	-0.397	-0.77	-1.17	-2.88	µs
		ISL706AEH/BEH/CEH	-0.35	-0.782	-1.516	-2.087	µs

Post Radiation Characteristics Unless otherwise specified, V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = +25°C. **This data is typical mean test data post radiation exposure at a rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed**

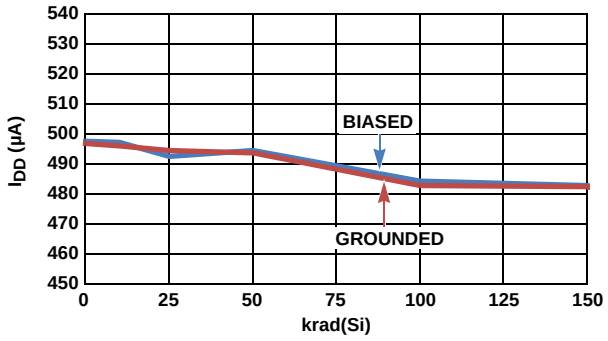


FIGURE 14. ISL705xEH I_{DD} vs LOW DOSE RATE RADIATION

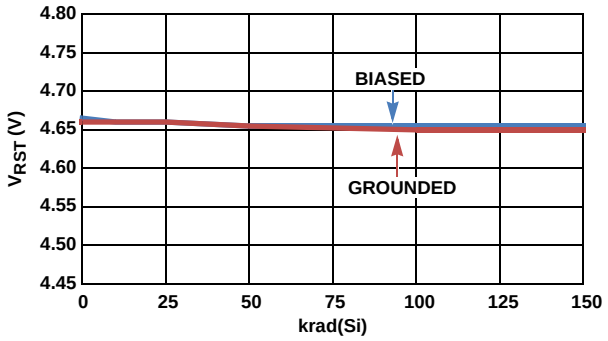


FIGURE 15. ISL705xEH V_{RST} vs LOW DOSE RATE RADIATION

Post Radiation Characteristics Unless otherwise specified, V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = +25°C. **This data is typical mean test data post radiation exposure at a rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed**

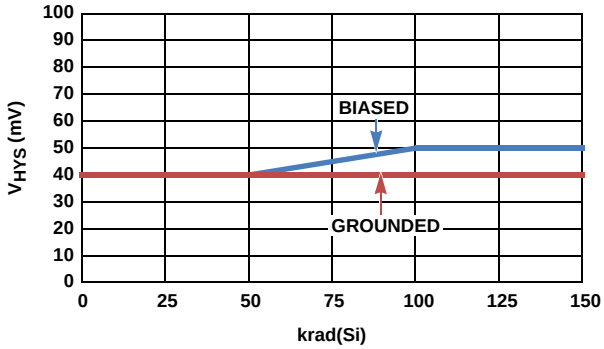


FIGURE 16. ISL705xEH V_{HYS} vs LOW DOSE RATE RADIATION

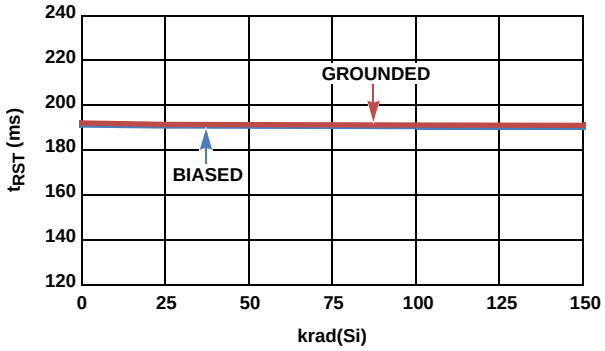


FIGURE 17. ISL705xEH t_{RST} vs LOW DOSE RATE RADIATION

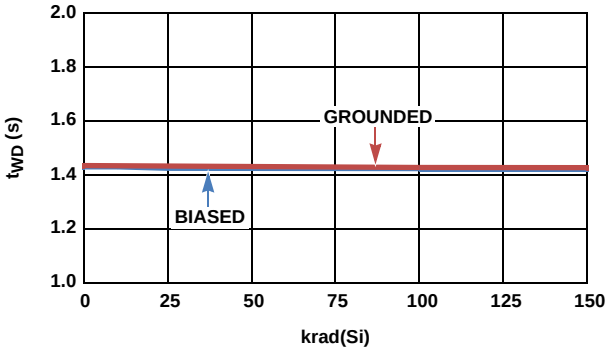


FIGURE 18. ISL705xEH t_{WD} vs LOW DOSE RATE RADIATION

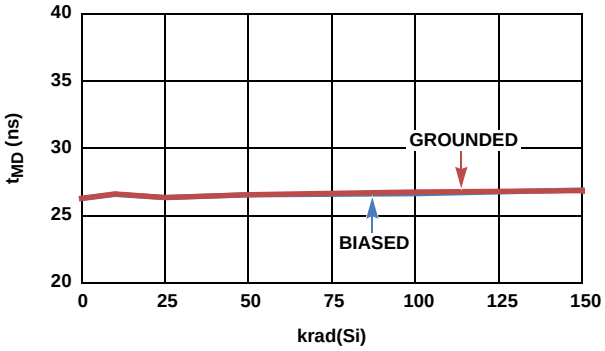


FIGURE 19. ISL705xEH t_{MD} vs LOW DOSE RATE RADIATION

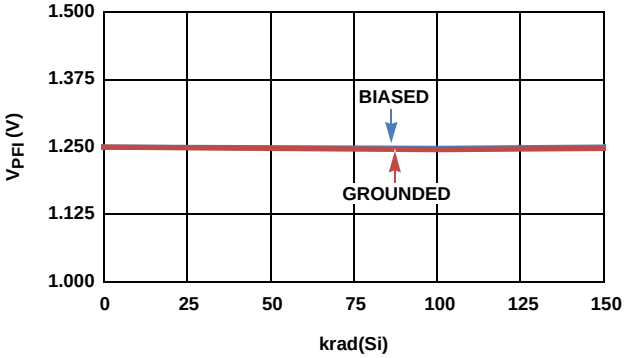


FIGURE 20. ISL705xEH V_{PFI} vs LOW DOSE RATE RADIATION

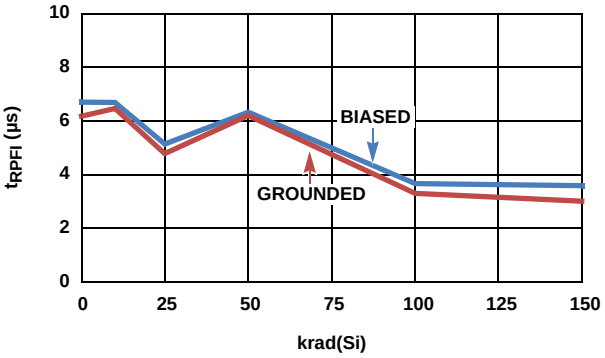


FIGURE 21. ISL705xEH t_{RPFI} vs LOW DOSE RATE RADIATION

Post Radiation Characteristics Unless otherwise specified, V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = +25°C. **This data is typical mean test data post radiation exposure at a rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed**

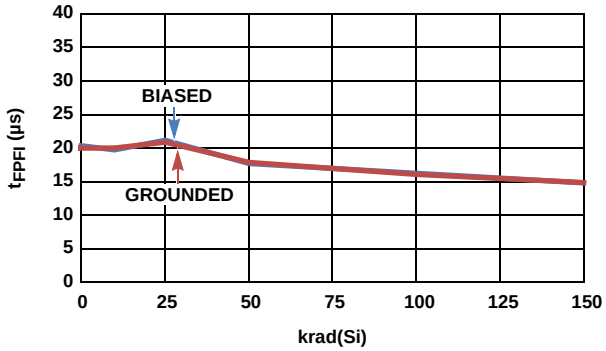


FIGURE 22. ISL705xEH t_{FPFI} vs LOW DOSE RATE RADIATION

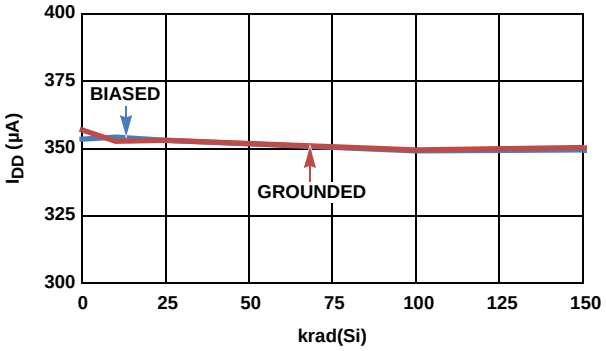


FIGURE 23. ISL706xEH I_{DD} vs LOW DOSE RATE RADIATION

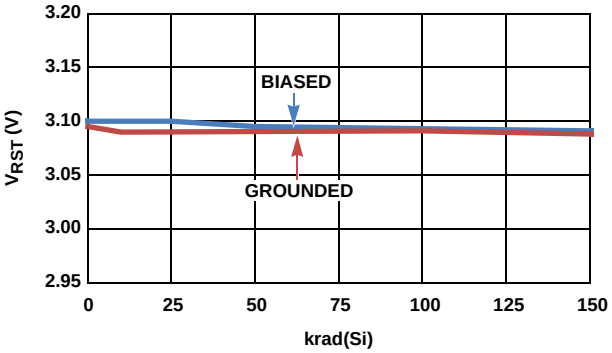


FIGURE 24. ISL706xEH V_{RST} vs LOW DOSE RATE RADIATION

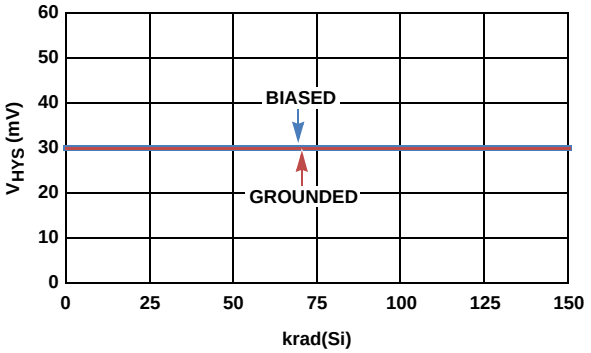


FIGURE 25. ISL706xEH V_{HYS} vs LOW DOSE RATE RADIATION

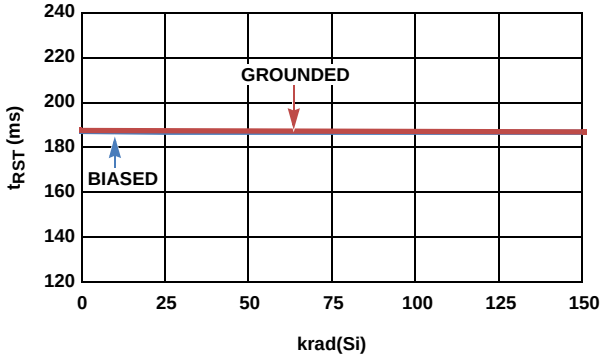


FIGURE 26. ISL706xEH t_{RST} vs LOW DOSE RATE RADIATION

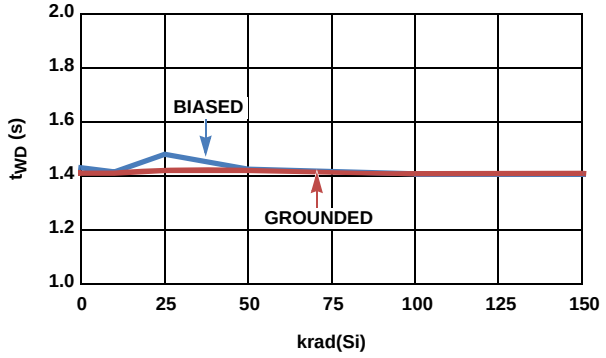


FIGURE 27. ISL706xEH t_{WD} vs LOW DOSE RATE RADIATION

Post Radiation Characteristics Unless otherwise specified, V_{DD} = 4.75V to 5.5V for the ISL705AEH/BEH/CEH, V_{DD} = 3.15V to 3.6V for the ISL706AEH/BEH/CEH T_A = +25°C. **This data is typical mean test data post radiation exposure at a rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed**

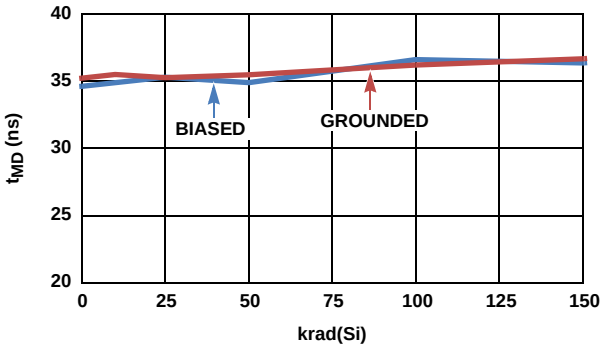


FIGURE 28. ISL706xEH t_{MD} vs LOW DOSE RATE RADIATION

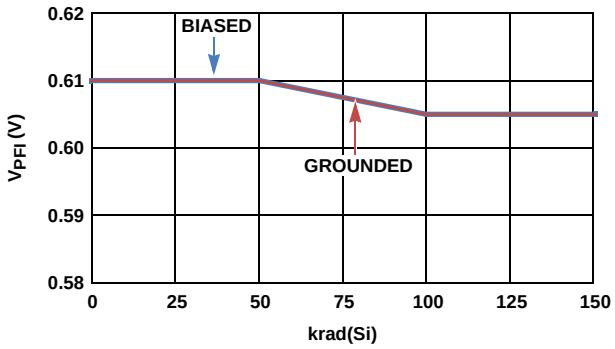


FIGURE 29. ISL706xEH V_{PFI} vs LOW DOSE RATE RADIATION

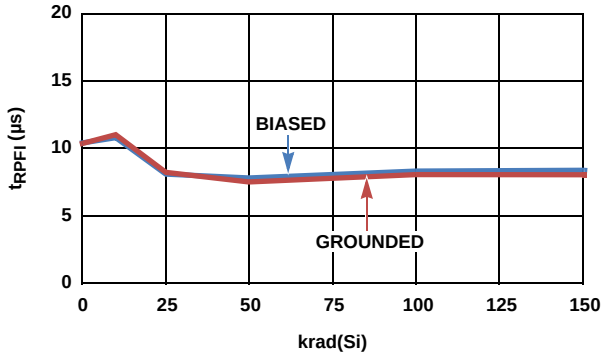


FIGURE 30. ISL706xEH t_{RPFI} vs LOW DOSE RATE RADIATION

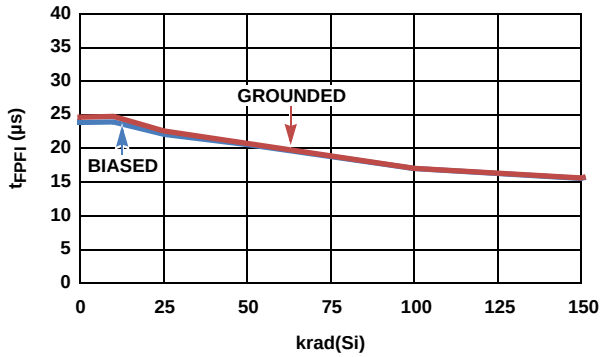


FIGURE 31. ISL706xEH t_{FPFI} vs LOW DOSE RATE RADIATION

Functional Overview

The ISL705xEH and ISL706xEH provide the functions needed for monitoring critical voltages in high reliability applications, such as microprocessor systems. Functions of the these supervisors include power-on reset control, supply voltage supervisions, power-fail detection, manual-reset assertion and a watch dog timer. The integration of all these functions along with their high threshold accuracy, low power consumption, and radiation tolerance make these devices ideal for critical supply monitoring.

Reset Output

Reset control has long been a critical aspect of embedded control design. Microprocessors require a reset signal during power up to ensure that the system environment is stable before initialization.

The reset signal provides several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are initialized.
- It allows time for an FPGA to perform its self configuration prior to initialization of the circuit.

On power-up, once V_{DD} reaches 1.2V, $\overline{RST}$ is guaranteed logic low. As V_{DD} rises, $\overline{RST}$ stays low. When V_{DD} rises above the reset threshold (V_{RST}), an internal timer releases $\overline{RST}$ after 200ms (typ). $\overline{RST}$ pulses low whenever V_{DD} degrades to below V_{RST} (see Figure 3). If a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse is lengthened 200ms (typ).

On power-down, once V_{DD} falls below the reset threshold, $\overline{RST}$ stays low and is guaranteed to be low until V_{DD} drops below 1.2V.

The ISL705BEH and ISL706BEH active-high RST output is simply the complement of the $\overline{RST}$ output, and is guaranteed to be valid with V_{DD} down to 1.2V. The ISL705CEH and ISL706CEH active-low open-drain reset output is functionally identical to $\overline{RST}$.

Power Failure Monitor

Besides monitoring V_{DD} for reset control, these devices have a Power-Failure Monitor feature that supervises an additional critical voltage on the Power-Fail Input (PFI) pin. For example, the PFI pin could be used to provide an early power-fail warning, overvoltage detection or monitor a power supply other than V_{DD}. $\overline{PFO}$ goes low whenever PFI is less than V_{PFI}.

The threshold detector can be adjusted using an external resistor divider network to provide custom voltage monitoring for voltages greater than V_{PFI}, according to Equation 1 (see Figure 32).

$$V_{IN} = V_{PFI}\left(\frac{R1 + R2}{R2}\right) \quad \text{(EQ. 1)}$$

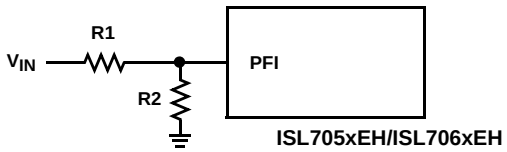


FIGURE 32. CUSTOM V_{TH} WITH RESISTOR DIVIDER ON PFI

Manual Reset

The manual reset input ($\overline{MR}$) allows designers to add manual system reset capability via a push button switch (see Figure 33). The $\overline{MR}$ input is an active low debounced input that asserts reset if the $\overline{MR}$ pin is pulled low to less than V_{IL} for at least 150ns. After $\overline{MR}$ is released, the reset output remains asserted for t_{RST} and then released. $\overline{MR}$ is a TTL/CMOS logic compatible, so it can be driven by external logic. By connecting $\overline{WDO}$ to $\overline{MR}$, one can force a watchdog time out to generate a reset pulse.

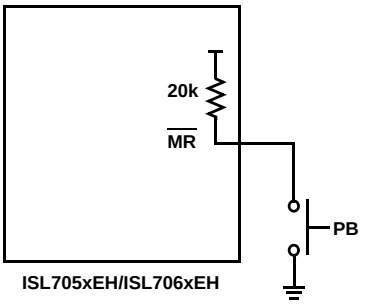


FIGURE 33. CONNECTING A MANUAL RESET PUSH-BUTTON

Watch Dog Timer

The watchdog time circuit checks for coherent program execution by monitoring the WDI pin. If the processor does not toggle the watchdog input within t_{WD} (1.0s min), $\overline{WDO}$ will go low. As long as reset is asserted or the WDI pin is tri-stated, the watchdog timer will stay cleared and not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected on the ISL705xEH, on ISL706xEH pulses as short as 100ns can be detected.

Whenever there is a low-voltage V_{DD} condition, $\overline{WDO}$ goes low. Unlike the reset outputs, however, $\overline{WDO}$ goes high as soon as V_{DD} rises above its voltage trip point (see Figure 4). With WDI open or connected to a tri-stated high impedance input, the Watchdog Timer is disabled and only pulls low when $V_{DD} < V_{RST}$.

Applications Information

Negative Voltage Sensing

This family of devices can be used to sense and monitor the presence of both a positive and negative rail. V_{DD} is used to monitor the positive supply while PFI monitors the negative rail. $\overline{PFO}$ is high when the negative rail degrades below a V_{TRIP} value and remains low when the negative rail is above the V_{trip} value. As the differential voltage across the R1, R2 divider is increased, the resistor values must be chosen such that the PFI node is <1.25V when the -V supply is satisfactory and the positive supply

is at its maximum specified value. This allows the positive supply to fluctuate within its acceptable range without signaling a reset when configured as shown in Figure 34.

$$R2 = \frac{R1(V_{PFI} - V_{TRIP})}{V_{DD} - V_{PFI}} \quad \text{(EQ. 2)}$$

In Figure 34, the ISL705AEH is monitoring +5V through V_{DD} and -5V through PFI. In this example, the trip point (V_{TRIP}) for the negative supply rail is set for -4.5V. Equation 2 can be used to select the appropriate resistor values. R1 is selected arbitrarily as 100kΩ, V_{DD} = 5V, V_{PFI} = 1.25V, and V_{TRIP} = (-4.5V). By plugging the values into Equation 2 (as shown in Equation 3) it can be seen a resistor of 153.3kΩ is needed. The closest 1% resistor value is 154kΩ.

$$R2 = \frac{100k(1.25 - (-4.5))}{5 - 1.25} = 153.3k\Omega \quad \text{(EQ. 3)}$$

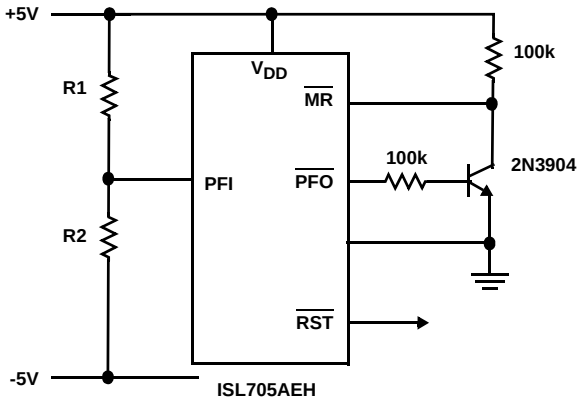


FIGURE 34. ±5V MONITORING

Figure 4 also has a general purpose NPN transistor in which the base is connected to the $\overline{PFO}$ pin through a 100kΩ resistor. The emitter is tied to ground and the collector is tied to $\overline{MR}$ signal. This configuration allows the negative voltage sense circuit to initiate a reset if it is not within its regulation window. A pull-up on the $\overline{MR}$ ensures no false reset triggering when the negative voltage is within its regulation window.

Assuring a Valid $\overline{RST}$ Output

When V_{DD} falls below 1.2V, the $\overline{RST}$ output can no longer sink current and is essentially an open circuit. As a result, this pin can drift to undetermined voltages if left undriven. By adding a pull-down resistor to the $\overline{RST}$ pin as shown in Figure 35, any stray charge or leakage currents will be drained to ground and keep $\overline{RST}$ low when V_{DD} falls below 1.2V. The resistor value (R1) is not critical however, it should be large enough not to load $\overline{RST}$ and small enough to pull $\overline{RST}$ to ground. A 100kΩ resistor would suffice, assuming there is no load on the $\overline{RST}$ pin during that time.

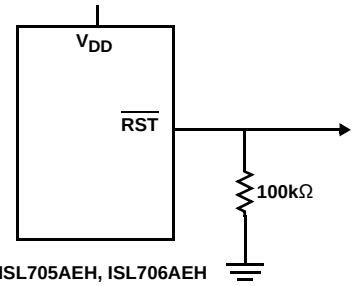


FIGURE 35. $\overline{RST}$ VALID TO GROUND CIRCUIT

Assuring a Valid RST Output

On the ISL705BEH and ISL706BEH, when V_{DD} falls below 1.2V, the RST output can no longer source enough current to track V_{DD}. As a result, this pin can drift to undetermined voltages if left undriven. By adding a pull-up resistor to the RST pin as shown in Figure 36, RST will track V_{DD} below 1.2V. The resistor value (R1) is not critical however, it should be large enough not to exceed the sink capability of RST pin at 1.2V. A 300kΩ resistor would suffice, assuming there is no load on the RST pin during that time.

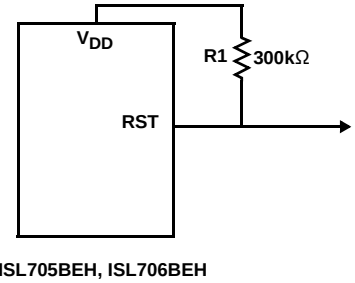


FIGURE 36. RST VALID TO GROUND CIRCUIT

Selecting Pull-Up Resistor Values

The ISL705CEH and ISL706CEH have open drain active low reset outputs ($\overline{RST\_OD}$). A pull-up resistor is needed to ensure $\overline{RST\_OD}$ is high when V_{DD} is in a valid state (Figure 37). The resistor value must be chosen in order not to exceed the sink capability of the $\overline{RST\_OD}$ pin. The ISL705AEH has a sink capability of 3.2mA and the ISL706CEH has a sink capability of 1.2mA. Equation 4 may be used to select resistor R_{PULL} based on the pull-up voltage V_{PULL}. It is also important that the pull-up voltage does not exceed V_{DD}.

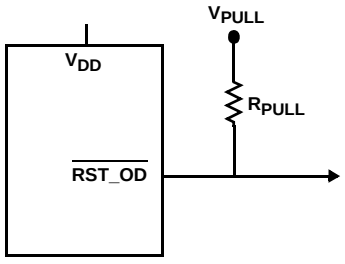


FIGURE 37. $\overline{RST\_OD}$ PULL-UP CONNECTION

$$R_{PULL} = \frac{V_{PULL}}{I_{SINK}} \quad \text{(EQ. 4)}$$

Adding Hysteresis to the PFI Comparator

The PFI comparator has no built in hysteresis, however the designer may add hysteresis by connecting a resistor from the $\overline{PFO}$ pin to the PFI pin, essentially adding positive feedback to the comparator (see Figure 38).

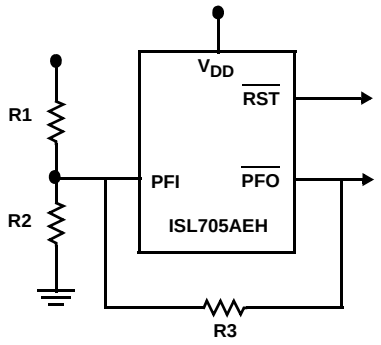


FIGURE 38. POSITIVE FEEDBACK FOR HYSTERISIS

The following procedure allows the system designer to calculate the components based on the requirements and on given data, such as supply rail voltages, hysteresis band voltage (V_{HB}), and reference voltage (V_{PFI}).

The comparator only has two states of operation. When it is low, the current through R3 is $I_{R3} = V_{PFI}/R3$. When the output is high, $I_{R3} = (V_{DD} - V_{PFI})/R3$. The feedback current needs to be very small so it does not induce oscillations; 200nA is a good starting point. Now two values of R3 can be calculated with V_{DD} = 5V and V_{PFI} = 1.25V; R3 = 6.25MΩ or 11.25MΩ, select the lowest value of the two.

With R3 selected as 6.2MΩ (closest standard 1% resistor), R1 can be calculated as:

$$R1 = R3\left(\frac{VHB}{V_{DD}}\right) = 124k\Omega \quad \text{(EQ. 5)}$$

with VHB selected at 100mV. The closest standard value for R1 is 124kΩ. Then next step is select the rising trip voltage (VTR) such that:

$$VTR > V_{PFI}\left(1 + \frac{VHB}{V_{DD}}\right) \quad \text{(EQ. 6)}$$

The rising threshold voltage is selected at 3.0V and R2 is calculated by Equation 7.

$$R2 = 1/\left[\left(\frac{VTR}{(V_{PFI} \times R1)}\right) - \left(\frac{1}{R1}\right) - \left(\frac{1}{R3}\right)\right] \quad \text{(EQ. 7)}$$

Plugging in all the variables R2 in this example is 90.9kΩ again this is choosing the closest 1% resistor. The final step is verify the trip voltages.

$$VTR = (V_{PFI}) \times R1\left[\left(\frac{1}{R1}\right) + \left(\frac{1}{R2}\right) + \left(\frac{1}{R3}\right)\right] \quad \text{(EQ. 8)}$$

$$VTF = VTR - \left(\frac{R1 \times VDD}{R3}\right) \quad \text{(EQ. 9)}$$

The rising voltage, VTR is calculated as 2.98V and the falling voltage VTF is calculated as 2.88V so 100mV hysteresis is achieved.

An additional item to consider is that the output voltage is equal to V_{DD}, however according to the “Electrical Specifications” on page 6, the output of the PFI comparator is guaranteed to be at least (V_{DD}-1.5) volts. When you take this worst case into account, the hysteresis can be as low at 70mV.

Special Application Considerations

Using good decoupling practices will prevent transients (i.e., due to switching noises and short duration droops in the supply voltage) from causing unwanted resets and reduce the power-fail circuit’s sensitivity to high-frequency noise on the line being monitored.

When the WDI input is left unconnected, it is recommended to place a 10µF capacitor to ground to reduce single event transients from arising in the $\overline{WDO}$ pin.

As described in the “Electrical Specifications” Table on page 7, there is a delay on the $\overline{PFO}$ pin whenever PFI crosses the threshold. This delay is due to internal filters on the PFI comparator circuitry which were added to mitigate single event transients. If the PFI input transitions below or above the threshold and the duration of the transition is less than the delay, the PFO pin will not change states.

Package Characteristics

Weight of Packaged Device

0.31 Grams typical

Lid Characteristics

Finish: Gold
Lid Potential: Unbiased
Case Isolation to Any Lead: 20 x 10^9 Ω (min)

Die Characteristics

Die Dimensions

2030µm x 2030µm (79.9 mils x 79.9 mils)
Thickness: 483µm ± 25.4µm (19.0 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ± 0.03µm to 1.2µm ± 0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7µm ±0.4µm

BACKSIDE FINISH

Silicon

PROCESS

0.6µM BiCMOS Junction Isolated

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased

ADDITIONAL INFORMATION

Worst Case Current Density

< 2 x 10^5 A/cm^2

Transistor Count

1400

Metallization Mask Layout

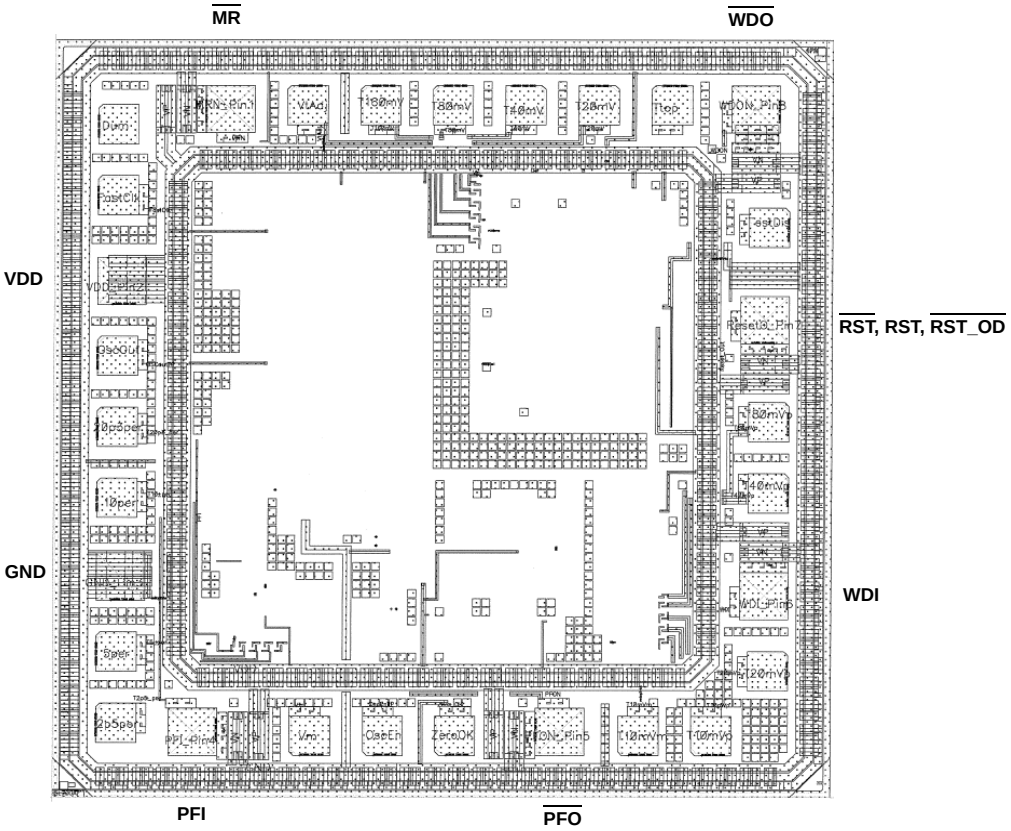


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
$\overline{MR}$	1	0	0	110	110	1
V_{DD}	2	-266.1	-435.35	110	110	1
GND	3	-266.1	-1184.75	110	110	1
PFI	4	-86.1	-1578	110	110	1
$\overline{PFO}$	5	818.85	-1578	110	110	1
WDI	6	1321.9	-1233.5	110	110	1
$\overline{RST}$, RST, $\overline{RST\_OD}$	7	1321.9	-534.05	110	110	1
$\overline{WDO}$	8	1297	0	110	110	1

NOTE:

8. Origin of coordinates is the centroid of pad 1.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 30, 2012	FN8262.0	Initial release

Products

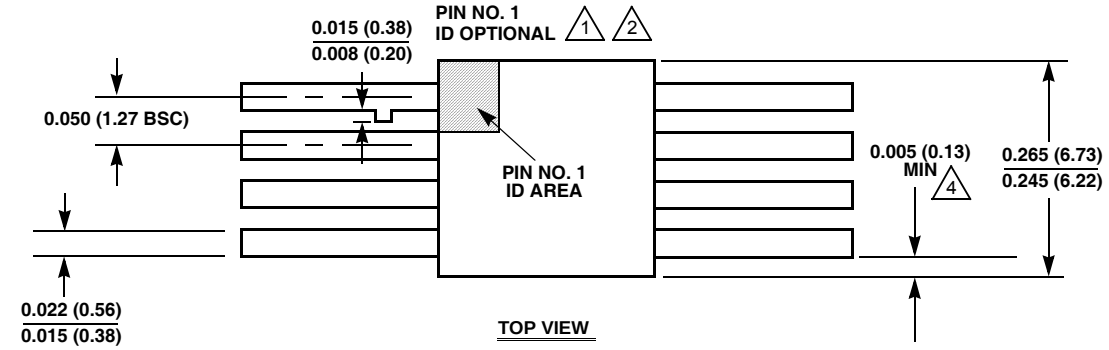
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

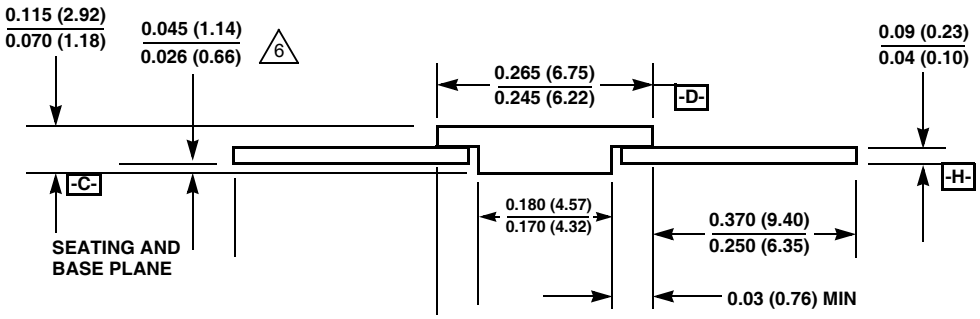
Package Outline Drawing

K8.A

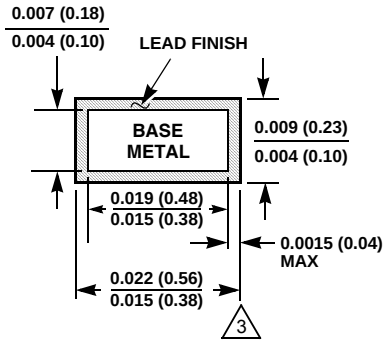
8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 12/10



TOP VIEW



SIDE VIEW



SECTION A-A

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.